ClickNP: Highly Flexible and High Performance Network Processing with Reconfigurable Hardware

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Challenge: FPGA programming

Hardware description languages: Verilog, VHDL…
Hard to program, hard to debug

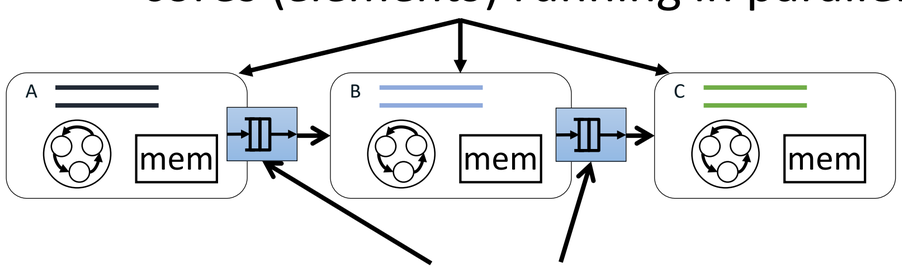
ClickNP: Making FPGA accessible to software developers

- **Flexible**: high-level language
- **Modular**: familiar Click abstractions
- **High performance**
- **Joint CPU/FPGA packet processing**

Programming model

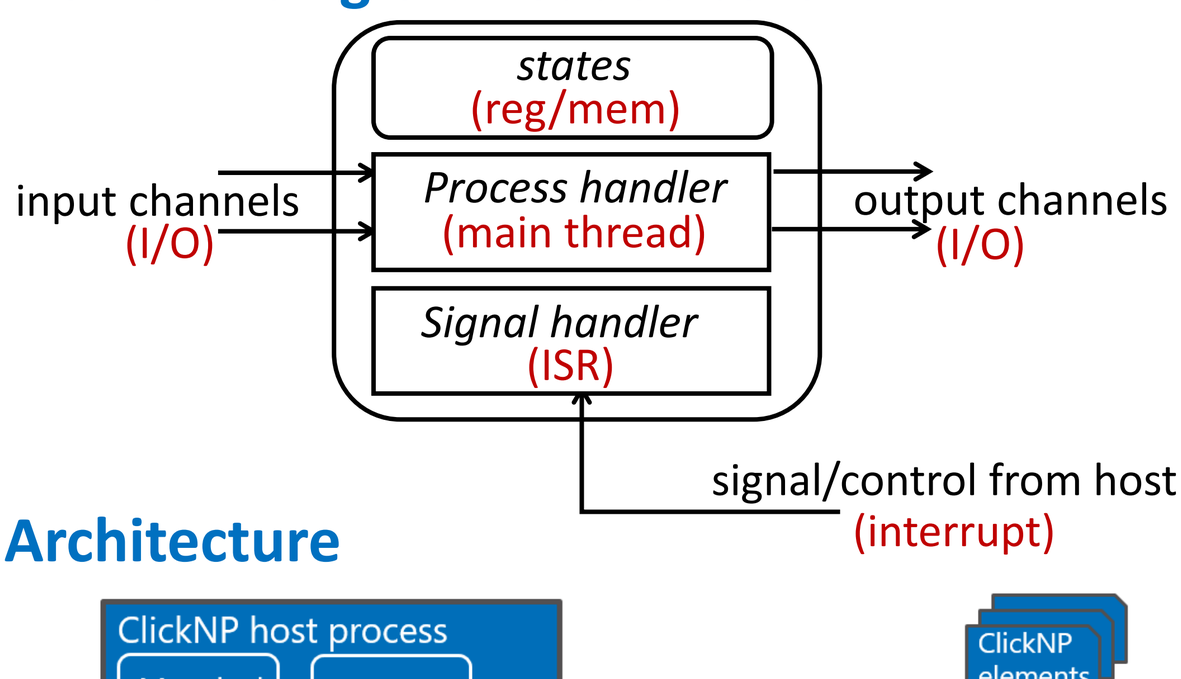
As if programming a **multi-core** processor

cores (*elements*) running in parallel

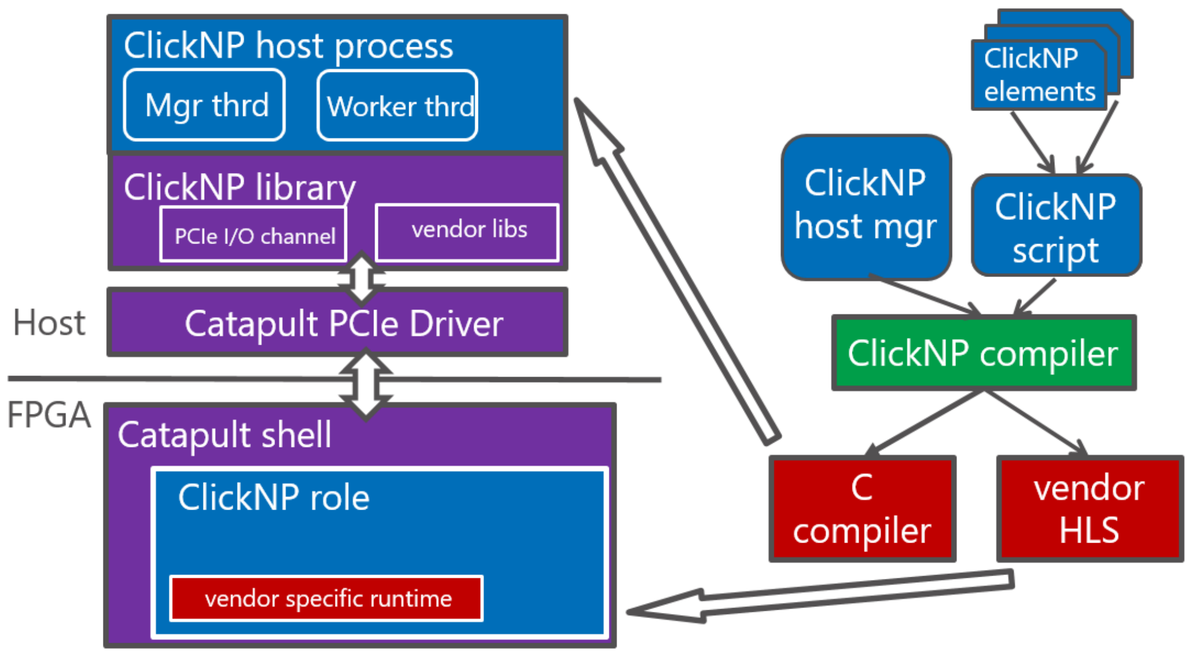


communicate via *channels*, not shared memory

Element: single-threaded core

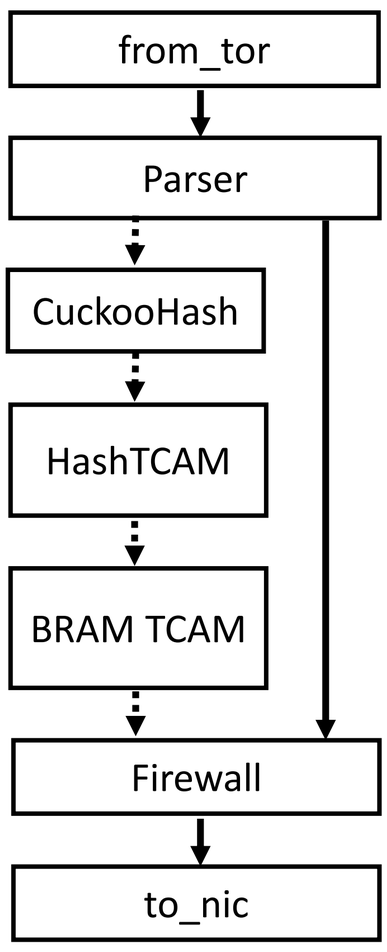


Architecture



Demo 1: Openflow firewall

Lookup table	Match type	Flow entries	Resource	
			Logic	BRAM
CuckooHash	Exact	64K	2%	34%
HashTCAM	16 masks	16 x 1K	19%	22%
BRAM TCAM	Full wildcard	1K	9%	23%



40 Gbps / 56 Mpps line rate
1.23 µs packet forward latency
<10 µs rule update latency

FW Cmd: {add,del}
nw_src nw_dst nw_proto
tcp_src tcp_dst
action={accept,drop}
priority

Demo 2: Stateful L4 load balancer